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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	13

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/519,695	KIM ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 13-22* is/are rejected.

7)☒ Claim(s) *3 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-6, 13-21, and newly added claim 22 have been considered. Claims 1-6 and 13 have been amended as per Applicant's request.

Claim Objections

2. Claim 3 is objected to because of the following informalities: Please correct the phrase "testing the set of control bits to identify *a* second prescribed condition" to read --testing the set of control bits to identify *the* second prescribed condition-- so that it is clear that the second prescribed condition being referred to is the one established in the first claim. Appropriate correction is required.

3. Claim 22 is objected to because of the following informalities: Please correct the phrase "expressly included subinstruction –*is* routed to multiple function processing units" to read -- expressly included subinstruction *is* routed to multiple function processing units--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 13-17, and 22 rejected under 35 U.S.C. 102(e) as being taught by Nishioka et al., U.S. Patent Number 6,401,190 (herein referred to as Nishioka).

6. Referring to claim 1, Nishioka has taught a method for sharing a subinstruction of a given VLIW instruction among functional processing units of a plurality of clusters on a processor having a very long instruction word architecture (Nishioka column 1, lines 41-57 and column 2, lines 51-67), the given VLIW instruction including a set of control bits and at least one subinstruction (Nishioka column 3, line 9-40 and Figure 3), the processor comprising the plurality of clusters (Nishioka column 10, line 64 to column 11, line 31 and Figure 1), each one cluster of the plurality of clusters comprising a plurality of functional processing units (Nishioka column 10, line 64 to column 11, line 31 and Figure 1), the plurality of functional processing units executing the given VLIW instruction (Nishioka column 10, line 64 to column 11, line 31; Figure 1; and Figure 2), the method comprising the steps of:

a. Testing the set of control bits of the given VLIW instruction to identify a prescribed condition for sharing a subinstruction within the given VLIW instruction among multiple functional processing units (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

b. When the prescribed condition is identified as a first prescribed condition, routing said shared subinstruction of the given VLIW instruction to multiple functional processing units as determined by the first prescribed condition (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

c. When the prescribed condition is identified as a second prescribed condition, routing said shared subinstruction of the given VLIW instruction to multiple

functional processing units as determined by the second prescribed condition, wherein the routing for the second prescribed condition is different than for the first prescribed condition (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7); and

d. Concurrently executing the subinstruction at said multiple functional processing units (Nishioka column 3, lines 9-40; column 10, line 64 to column 11, line 31; column 13, lines 12-51; Figure 1; Figure 5; and Figure 6).

7. Referring to claim 2, Nishioka has taught in which the step of routing comprises routing said shared subinstruction of the given VLIW instruction to a first functional processing unit of a first cluster of the plurality of clusters and to a first functional processing unit of a second cluster of the plurality of clusters; and in which the step of executing comprises concurrently executing; the shared subinstruction at said first functional processing unit of the first cluster of the plurality of clusters and at the first functional processing unit of the second cluster of the plurality of clusters (Nishioka column 10, line 64 to column 11, line 31; column 12, line 62 to column 14, line 5; column 15, line 43 to column 16, line 12; Figure 1; Figure 2; and Figure 7).

8. Referring to claim 3, Nishioka has taught in which the given VLIW instruction comprises a first subinstruction and a second subinstruction (Nishioka column 3, lines 9-40 and Figure 3), the step of testing comprising testing the set of control bits to identify a first prescribed condition, the step of routing comprising routing the first subinstruction (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7), the method further comprising the steps of:

a. Testing the set of control bits to identify the second prescribed condition (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

b. Then the second prescribed condition is identified, routing said second subinstruction of the given instruction to a second functional processing unit of the first cluster of the plurality of clusters and to a second functional processing unit of the second cluster of the plurality of clusters (Nishioka column 10, line 64 to column 11, line 31; column 12, line 62 to column 14, line 5; column 15, line 43 to column 16, line 12; Figure 1; Figure 2; and Figure 7); and

c. Concurrently executing the subinstruction at the first functional processing unit and the second functional processing unit (Nishioka column 3, lines 9-40; column 10, line 64 to column 11, line 31; column 13, lines 12-51; Figure 1; Figure 5; and Figure 6); and

d. Wherein the step of executing comprises concurrently executing the first subinstruction at the first functional processing unit of the first cluster, the first subinstruction at the first functional processing unit of the second cluster, the second subinstruction at the second functional processing unit of the first cluster and the second subinstruction at the second functional processing unit of the second cluster (Nishioka column 3, lines 9-40; column 10, line 64 to column 11, line 31; column 13, lines 12-51; Figure 1; Figure 5; and Figure 6).

9. Referring to claim 4, Nishioka has taught a method for storing an a VLIW instruction of a computer program to be executed on a processor having a very long instruction word architecture,

a. Wherein each VLIW instruction comprises at least one subinstruction and up to a first prescribed number of subinstructions, the first prescribed number being at least two (Nishioka column 3, lines 9-40; column 14, lines 6-24; and Figure 3),

b. Wherein the processor is organized into a plurality of clusters equaling a second prescribed number (Nishioka column 10,line 64 to column 11, line 31 and Figure 1), each one cluster of the plurality of clusters comprising a common number of functional processing units (Nishioka column 10, line 64 to column 11, line 31 and Figure 1), wherein the common number of functional processing units times the second prescribed number equals the first prescribed number (Nishioka column 13, lines 21-24; column 14, lines 9-24; Figure 1; and Figure 3),

c. Wherein for a given instruction having the first prescribed number of subinstructions, each functional processing unit of the plurality of clusters is for executing a respective subinstruction of the given instruction (Nishioka column 10, line 64 to column 11, line 31; Figure 1; and Figure 2), the method comprising, during compilation of the computer program, the steps of:

i. Identifying a pattern in which a subinstruction occurs more than once in the given instruction, said subinstruction being a redundant subinstruction (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56;

column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7)

ii. Determining whether the pattern is among a set of prescribed patterns (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

iii. When the pattern is among the set of prescribed patterns, setting a set of control bits for the instruction to indicate that said pattern is present (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7).

10. Referring to claim 13, Nishioka has taught a computer system comprising:

a. A processor having a very large word instruction architecture (Nishioka column 1, lines 41-57 and column 2, lines 51-67) and including a plurality of clusters of functional processing units (Nishioka column 10, line 64 to column 11, line 31 and Figure 1), each one cluster of the plurality of clusters comprising a common number of functional processing units (Nishioka column 10, line 64 to column 11, line 31 and Figure 1), the processor comprising a first prescribed number of clusters (Nishioka column 10, line 64 to column 11, line 31 and Figure 1), said very large word instruction architecture allowing an instruction to have up to a second prescribed number of subinstructions (Nishioka column 3, lines 9-40; column 14, lines 6-24; and Figure 3), where the second prescribed number equals

the first prescribed number times the common number (Nishioka column 13, lines 21-24; column 14, lines 9-24; Figure 1; and Figure 3), each instruction to be executed by the processor comprising from one subinstruction up to the second prescribed number of subinstructions, along with a set of control bits (Nishioka column 10, line 64 to column 11, line 31; Figure 1; and Figure 2); and

b. An instruction cache memory which stores a first VLIW instruction (Nishioka column 10, line 64 to column 11, line 31; column 14, lines 6-24 and 38-56; Figure 1; Figure 3; and Figure 6) in a compressed format determined by a condition of the set of control bits, the compressed format including a shared subinstruction stored in a given field of the first VLIW instruction which is to be shared by a plurality of the functional processing units, said plurality of functional processing units being determined by said condition of the. set of control bits (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7).

11. Referring to claim 14, Nishioka has taught in which said shared subinstruction is for a first functional processing unit of a first cluster and a first functional processing unit of a second cluster when the set of control bits identifies a first prescribed condition (Nishioka column 10, line 64 to column 11, line 31; column 12, line 62 to column 14, line 5; column 15, line 43 to column 16, line 12; Figure 1; Figure 2; and Figure 7).

12. Referring to claim 15, Nishioka has taught in which the shared subinstruction is shared subinstruction for a second functional processing unit of the first cluster and a second functional processing unit of the second cluster when the set of control bits either concurrently identifies a

second prescribed condition (Nishioka column 10, line 64 to column 11, line 31; column 12, line 62 to column 14, line 5; column 15, line 43 to column 16, line 12; Figure 1; Figure 2; and Figure 7).

13. Referring to claim 16, Nishioka has taught:

a. Means for testing the set of control bits for a given instruction (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7); and

b. Means for routing said first common subinstruction to the first functional processing unit of the first cluster and to the first functional processing unit of the second cluster of the plurality of clusters when said testing means identifies the first prescribed condition (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7).

14. Referring to claim 17, Nishioka has taught in which the first common subinstruction is concurrently executed at the first functional processing unit of the first cluster and the first functional processing unit of the second cluster (Nishioka column 3, lines 9-40; column 10, line 64 to column 11, line 31; column 13, lines 12-51; Figure 1; Figure 5; and Figure 6).

15. Referring to claim 22, Nishioka has taught a method for processing a compressed-length VLIW instruction on a processor having a very long instruction word architecture (Nishioka column 1, lines 41-57 and column 2, lines 51-67), the compressed-length VLIW instruction including a set of control bits and at least one subinstruction (Nishioka column 3, lines 9-40 and Figure 3), the processor comprising a plurality of clusters (Nishioka column 10, line 64 to

column 11, line 31 and Figure 1), each one cluster of the plurality of clusters comprising a plurality of functional processing units (Nishioka column 10, line 64 to column 11, line 31 and Figure 1), the method comprising the steps of:

a. Loading the compressed-length VLIW instruction into a cache (Nishioka column 10, line 64 to column 11, line 31; column 14, lines 6-21 and 38-56; Figure 1; Figure 3; and Figure 6);

b. Testing the set of control bits of the compressed-length VL1W instruction to determine distribution of the at least one subinstruction, wherein each one functional processing unit of the plurality of functional processing units of each cluster receives one of a no-operation subinstruction or a subinstructlon expressly included among the at least one subinstruction (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

c. Wherein for a first prescribed condition of the set of control bits, at least one expressly included subinstruction is routed to multiple functional processing units as determined by the first prescribed condition (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

d. Wherein for a second prescribed condition of the set of control bits, at least one expressly included subinstruction is routed to multiple functional processing units as determined by the second prescribed condition, wherein the routing for the second prescribed condition is different than for the first prescribed condition

(Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7); and

e. Executing the compressed-length VLIW instruction as distributed among the plurality of functional units of each cluster by concurrently executing the subinstructions received at the plurality of functional processing units of each cluster (Nishioka column 3, lines 9-40; column 10, line 64 to column 11, line 31; column 13, lines 12-51; Figure 1; Figure 5; and Figure 6).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 5-6 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al., U.S. Patent Number 6,401,190 (herein referred to as Nishioka), as applied to claims 1 and 14, in view of Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek).

18. Referring to claim 5, Nishioka has not taught during compilation of the computer program, compressing the given instruction when the pattern is among the set of prescribed patterns by deleting one occurrence and leaving unchanged another occurrence of the redundant subinstruction in the given instruction to achieve a compressed-length VLIW instruction and storing the compressed-length VLIW instruction as part of the compiled computer program; and

storing the compressed-length VLIW instruction as part of the compiled computer program. However, Nishioka has taught fetching compressed-length instructions that contain only one set of operations that would be executed by all functional units (Nishioka column 14, lines 6-24 and 38-56; Figure 3; and Figure 6). Pechanek has taught during compilation of the computer program, compressing the given instruction when the pattern is among the set of prescribed patterns by deleting one occurrence and leaving unchanged another occurrence of the redundant subinstruction in the given instruction to achieve a compressed-length VLIW instruction and storing the compressed-length VLIW instruction as part of the compiled computer program; and storing the compressed-length VLIW instruction as part of the compiled computer program (Pechanek column 3, lines 54-59). A person of ordinary skill in the art would have recognized that a compressed-length instruction optimizes efficiency and minimized the size for specific applications, thereby allowing more applications. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate compressed-length instructions of Pechanek in the device of Nishioka to improve processor storage efficiency.

19. Referring to claim 6, Nishioka has taught during run time of the computer program, the steps of:

a. Moving the compressed-length VLIW instruction into an instruction cache (Nishioka column 14, lines 6-24 and 38-56; Figure 3; and Figure 6). In regards to Nishioka, the instruction has to have been moved to the instruction memory, since the instruction is being fetched from the instruction memory and a cache is a type of memory.

b. Testing the set of control bits of the compressed-length VLIW instruction to determine a condition is identified in which subinstruction sharing is to occur for the compressed-length VLIW instruction (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

c. When subinstruction sharing is determined to occur, parsing the compressed-length VLIW instruction to route the redundant subinstruction to a plurality of functional processing units as determined by the identified condition (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

d. Concurrently executing the subinstruction at said plurality of functional (Nishioka column 3, lines 9-40; column 10, line 64 to column 11, line 31; column 13, lines 12-51; Figure 1; Figure 5; and Figure 6).

20. Referring to claims 18-21, Nishioka has taught:

a. In which the first instruction in an uncompressed format includes the second prescribed number of subinstructions, the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster, the system further comprising means for compiling the first instruction (Applicant's claim 18) (Nishioka column 13, lines 21-24; column 14, lines 9-24; Figure 1; and Figure 3), the compiling means

comprising means for setting a state of the set of control bits to identify a first prescribed condition when the first subinstruction is equal to the second subinstruction (Applicant's claim 18) (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7).

b. In which a first instruction in uncompressed format includes the second prescribed number of subinstructions, the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster, the system further comprising means for compressing the first instruction into the compressed format (Applicant's claim 19) (Nishioka column 13, lines 21-24; column 14, lines 9-24; Figure 1; and Figure 3), the compressing means comprising means for testing the set of control bits associated with the first instruction (Applicant's claim 19) (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

c. In which a first instruction in uncompressed format includes the second prescribed number of subinstructions, the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster, the system further comprising means for

caching the first instruction (Applicant's claim 20) (Nishioka column 13, lines 21-24; column 14, lines 9-24; Figure 1; and Figure 3), the caching means comprising:

i. Means for testing the set of control bits associated with the first instruction (Applicant's claim 20) (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56; column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

ii. Means for loading the first instruction into the instruction cache in the compressed format (Applicant's claim 20) (Nishioka column 10, line 64 to column 11, line 31; column 14, lines 6-21 and 38-56; Figure 1; Figure 3; and Figure 6).

d. The systems of claim 14, in which a first instruction in uncompressed format includes the second prescribed number of subinstructions, the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster, the system further comprising means for caching the first instruction (Applicant's claim 21) (Nishioka column 13, lines 21-24; column 14, lines 6-56; Figure 1; and Figure 3), the caching means comprising:

i. Means for setting a state of the set of control bits associated with the first instruction to identify a first prescribed condition when the first subinstruction is equal to the second subinstruction (Applicant's claim 21) (Nishioka column 12, line 52 to column 14, line 5; column 14, lines 6-56;

column 15, line 56 to column 16, line 12; Figure 2; Figure 3; Figure 5; Figure 6; and Figure 7);

ii. Means for loading the first instruction into the instruction cache in the compressed format (Applicant's claim 21) (Nishioka column 10, line 64 to column 11, line 31; column 14, lines 6-21 and 38-56; Figure 1; Figure 2; and Figure 6).

21. Nishioka has not taught

a. Means for comparing the first subinstruction and the second subinstruction (Applicant's claims 18 and 21);

b. Means for reducing the size of the first instruction by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Applicant's claim 19); and

c. Means for reducing the size of the first instruction to achieve a compressed format by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Applicant's claims 20 and 21).

22. However, Nishioka has taught fetching compressed-length instructions that contain only one set of operations that would be executed by all functional units (Nishioka column 14, lines 6-24 and 38-56; Figure 3; and Figure 6). Pechanek has taught:

a. Means for comparing the first subinstruction and the second subinstruction (Applicant's claims 18 and 21) (Pechanek column 3, lines 54-59);

b. Means for reducing the size of the first instruction by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Applicant's claim 19) (Pechanek column 3, lines 54-59); and

c. Means for reducing the size of the first instruction to achieve a compressed format by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Applicant's claims 20 and 21) (Pechanek column 3, lines 54-59).

23. A person of ordinary skill in the art would have recognized that a compressed-length instruction optimizes efficiency and minimized the size for specific applications, thereby allowing more applications. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate compressed-length instructions of Pechanek in the device of Nishioka to improve processor storage efficiency.

Response to Arguments

Applicant's arguments with respect to claims 1-6 and 13-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

26. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

November 30, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100